IN THE SPECIFICATION

Please insert on page 1, and immediately above the heading "BACKGROUND OF THE INVENTION", The following new heading and paragraph which are braced by double hyphens (--): [Clean copies of changed specification paragraphs are provided in the Appendix]

-- CROSS REFERENCE TO RELATED APPLICATIONS

The present application is a continuation of, and claims benefit of, U.S. Patent Application No. 10/071,689 filed February 8, 2002, whose entire disclosure is incorporated herein by reference. --

Please amend the paragraph on page 3, lines 11-18, as follows:

Fig. 2 illustrates a cross section of a nonvolatile memory cell at an early stage of fabrication. Semiconductor substrate 120 (monocrystalline silicon or some other material) is processed to form a suitably doped channel region 150 (type P in Fig. 2, but an N type channel can also be used). Dielectric 130 is formed on substrate 120 over channel 150. Dielectric 130 may be thermally grown silicon dioxide or some other type of dielectric. Then polysilicon layer 110 is deposited and doped during or after deposition. See for example U.S. patent application 09/640,139 filed August 15, 2000 and incorporated herein by reference **(now U.S. patent no. 6,355,524 issued March 12, 2002).**

Please amend the paragraph on page 5, lines 12-22, as follows:

Known techniques can be used to complete the memory fabrication. In the example of Fig. 4, silicon nitride layer 410 is formed by low pressure CVD (LPCVD) on layer 310. Silicon dioxide 420 is deposited by CVD, or thermally grown, on layer 410. Layers 310, 410, 420 are referenced as 160. Doped polysilicon 170, or some other conductive material, is deposited to provide the control gates (possibly wordlines each of which provides the control gates for a row of memory cells). The layers 170, 420, 410, 310, 110, 130 are patterned as needed. Source/drain regions 140 are formed by doping. Additional layers (not shown) may be formed to provide select gates, erase gates, or other features. See the aforementioned U.S. patent **no. 6,355,524 [application 09/640,139]** for an exemplary memory fabrication process that can be modified to incorporate the floating gate nitridation described above.

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